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| Serial No: |
| **Final Exam** |
| **Total Time: 3 Hour** |
| **Total Marks: MRKS** |
| \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Signature of Invigilator |

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| **EE-227 Computer**  **Logic Design** |
| Wednesday, June 17th , 2015 |
| **Course Instructor** |
| Dr. Ayub Alvi, Dr. Fuleah Razzak and  Mr. Jawad Hassan |

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| **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**  Student NameRoll No Section Signature |
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## DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

**Instructions:**

1. Attempt on question paper. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
2. No additional sheet will be provided for rough work. Use and mark the back of the last page for rough work.
3. If you need more space write on the back side of the paper and clearly mark question and part number etc.
4. After asked to commence the exam, please verify that you have **16 pages** different printed pages including this title page. There are total of **4 Questions**.
5. **Calculator is NOT allowed**.
6. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.
7. **For each question show your complete method in solution**.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Q-1** | **Q-2** | **Q-3** | **Q-4** | **Total** |
| **Total**  **Marks** | **30** |  |  | **35** |  |
| **Marks Obtained** |  |  |  |  |  |

**Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Question # 1[3 + 3 + 6 + 6 + 6 +6 = 30]**

1. Reduce the following expression to three literals. [3]

**A'C' + ABC + AC'**

1. Convert (776.625)8 to binary and then convert the resulting binary number to hexadecimal. Show your method. [3]
2. Using two (2 x 4) decoders, enable and external gates design a combinational circuit defined by following two functions. [6]
3. F1(x,y,z) = ( y + z*'* )x’
4. F2(x,y,z) = ∑(1, 3, 4, 5)
5. Implement following function with a 4x1 multiplexer. [6]

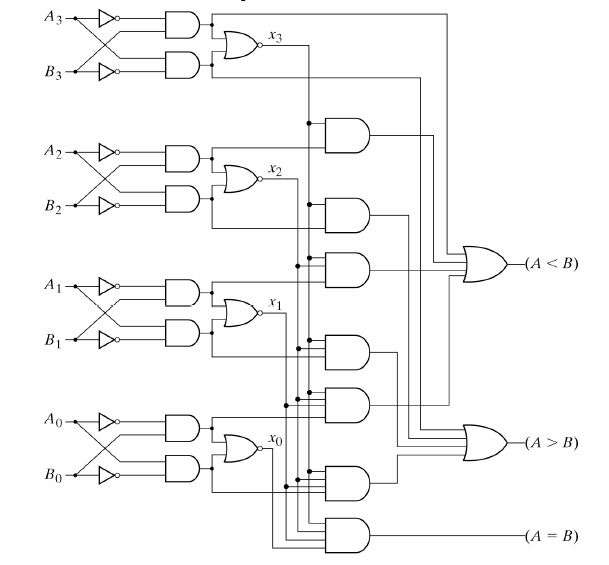
F(A,B,C,D) = ∑(0,2,3,6,9,12,14,15)

1. A 4-bit magnitude comparator circuit is shown below: [6]

Give the expression for F(A<B). Label the output of all gates when comparing two numbers

A = 1000

B = 1010



1. Design a 4-bit priority encoder with following priority sequence. [6]

**D2 < D0 < D3 < D1**

**Question # 2[4 + 9 + 10 + 12 = 35]**

1. Draw and label the circuit diagram of a positive edge triggered D-flip flop in master slave configuration using two D latch blocks. [4]
2. A sequential circuit with two D flip flops, A and B; two inputs, x and y; and one output z, is specified by the following next state and output equations:

A (t+1) = x’y + xA’

B (t+1) = xB + y’A

z = B+x’y

1. Draw the logic diagram of the circuit. [3]
2. List the state table for the sequential circuit. [3]
3. Draw the corresponding state diagram. [3]
4. Analyze the following circuit with JK flip flops and provide the flip flop input equations, state table and state diagram. [10]

1. Design a sequential circuit using T flip-flop by using following State transition diagram. Treat unused states as don’t cares. [12]



**Question # 3[10 + 12 + 8 + 10 = 40]**

1. Design a two-bit counter using JK flip-flops which has one input x. [10]

When x=0, the counting sequence is 11, 01, 00, 10 and repeats.

When x=1, the counting sequence is 01, 11, 10, 00 and repeats.

1. Design a 4 bit Modulo-9 counter (i.e. the counter goes up till 8 only and then goes back to 0). Clearly show all the design steps. Use only T-flip flops. Only diagrams as solution to this question are not acceptable. [12]

**Note**: Treat unused states as don’t cares.

1. Draw and label the circuit diagram of a universal shift register using four 4 x 1 multiplexers and four D flip flops. The shift register should operate according to the following table. [8]

|  |  |  |
| --- | --- | --- |
| **S1** | **S0** | **Operation** |
| 0 | 0 | Reset to 0 |
| 0 | 1 | Shift left |
| 1 | 0 | Parallel Load |
| 1 | 1 | Complement the input |

1. Students of Batch BSCS-2012 have developed a new flip-flop named LM Flip-Flop. When inputs of L and M are 00, 01, 10 and 11, the flip-flop is cleared to zero, complements, sets to 1, and no change occurs respectively. For LM Flip-Flop: [10]
   1. Tabulate its characteristic table
   2. Tabulate excitation table
   3. Derive its excitation table
   4. Construct D-type Flip-Flop using LM flip-flop.

**Question # 4[15 + 10 + 10 = 35]**

1. Implement the following functions using a PLA with minimum number of product terms. construct PLA table and draw and label the PLA diagram clearly showing all the connections. [15]

F1 (w,x,y,z) = Σ (2, 3, 4, 5, 6, 7, 10, 11)

F2 (w,x,y,z) = Σ (1, 3, 9, 11, 12, 13, 15)

F3 (w,x,y,z) = Σ (1, 4, 6, 7, 9, 12, 14, 15)

F4 (w,x,y,z) = Σ (0, 2, 5, 7, 8, 10, 13, 15)

1. Implement the following functions using the PAL. Construct PAL table and draw PAL diagram. [10]

NOTE: Functions are treated as simplified.

W(A,B,C,D) = ABC’ +B’CD’

X (A,B,C,D) = A + BD

Y(A,B,C,D) = ABC’ + B’CD’ + AC’D’ + A’B’C’D

Z (A,B,C,D) = A’B + CD + B’D’

1. Implement following functions using 16 X 4 ROM. Give the ROM table and Draw the circuit. [10]

F1 (A,B,C,D) = A' C' + B' D' + ABC

F2 (A,B,C,D) = B' C + ACD + A' B C'

F3 (A,B,C,D) = C' D' + CD + A' BC + AC' D'

F4 (A,B,C,D) = BC' + BCD' + ABC